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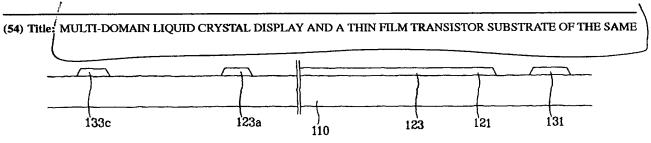
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(57) Abstract: A thin film transistor array panel is provided, which includes; an insulating substrate; a plurality of gate lines formed on the insulating substrate; a plurality of data lines formed on the insulating substrate, insulated from the gate lines, and intersecting the gate lines; a plurality of storage electrode lines formed on the insulating substrate, insulated from the data lines, and intersecting the data lines; a plurality of pixel electrodes provided on the respective pixel areas defined by the intersections of the gate lines and the data lines, each pixel electrode having a cutout; a plurality of direction control electrodes provided on the respective pixel areas defined by the intersections of the gate lines and the data lines; a first thin film transistor connected to a relevant one of the gate lines, a relevant one of the data lines and a relevant one of the gate lines, a relevant one of the data lines and a relevant one of the gate lines, a previous one of the data lines and a relevant one of the data lines and a relevant one of the data lines and a relevant one of the direction control electodes; an a third thin film transistor connected to the previous gate line, the relevant data line and the relevant pixel electrode.